REMARKS

This paper is being provided in response to the February 7, 2002 Office Action for the above-referenced application. In this response, applicant has amended claims 1 and 6 in order to more particularly point out and distinctly claim that which applicant deems to be the invention. Applicant respectfully submits that the amendments to the claims are supported by the originally filed specification. Specifically, the surrounding of the second S/D regions by the first is found at least on page 11 of the specification.

In response to the objection to claims 6 and 22, applicant has amended claims 6 to clarify that the independent claim recites one or more sidewalls that have a lateral extent greater than the thickness of the film, that is there is a horizontal portion of the film rather than just a sidewall film. Thus, the dependent claim disclosure of only one sidewall presents no difficulty, since the conductive wiring may be determined by the sidewall or the offset. Applicant believes that this amendment clarifies the meaning of the claims, and is fully responsive to the objection set forth in the Office Action. Accordingly, applicant respectfully requests that this objection be withdrawn.

The rejection of claims 1-11 and 20-23 under 35 U.S.C. 112, first paragraph, as containing subject mater not described in the specification in such a way as to reasonably convey to one skilled in the art that the inventor had possession of the claimed invention, has been addressed by the claims amendments contained herein. Specifically, the claims language of one of the source and drain regions extending towards the gate electrode has

been removed from the independent claims. Accordingly, applicant respectfully requests that this objection be withdrawn.

The rejection of claims 1, 5 and 20 under 35 U.S.C. 103(a) as being obvious over Gonzales (U.S. Patent No. 5,39, 835, hereinafter referred to as "Gonzales") is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that claims1, 5 and 20, as amended herein, are neither disclosed nor suggested by the cited reference of Gonzales.

Applicant's claim 1, as amended herein, recites a semiconductor device having a substrate, and an insulating film formed at a surface of the substrate for defining device regions in each of which a semiconductor device is to be fabricated. There is a gate electrode formed on the substrate, and first drain and source diffusion layers formed at a surface of the substrate around the gate electrode. There is at least one sidewall that covers the gate electrode and extends laterally. There are second drain and source diffusion layers formed at a surface of the substrate surround the first drain and source electrodes. The sidewall has a sidewall offset extending outwardly of the gate electrode along a surface of the substrate in at least one region below which the drain and source diffusion layers are formed. The sidewall offset extends along a surface of a gate oxide film on which the gate electrode is formed by more than the thickness of the sidewall. At least one of the drain and source diffusion layers extend towards the gate electrode beyond an edge of the sidewall offset. Claim 5 depends from claim 1 and adds the feature of a memory cell.

The cited reference of Gonzales discloses a process for fabricating a CMOS dynamic random access memory. This process uses a high energy ion implantation of boron ions that is performed at a oblique angle for punch through protection. Figure 9, and the associated portions of the specification, disclose metal 92 connected to the graded junction 24B formed by the oblique implantation. The metal 92 is remote from peripheral edge of the sidewall offset. There are also disclosed metal lines 51 that are directly upon the sidewall film.

The cited reference of Gonzales does not have a sidewall film that extends laterally away from the gate by an amount greater than the thickness of the sidewall, as recited in the present independent claims, and further does not use the sidewall as part of the definition of the surrounded drain and source regions. The cited figure 9 especially shows this point, since the cited drain near region 13 is clearly defined by the gate electrode 16, rather than the unlabeled sidewall film.

By contrast, the present application discloses a double diffused drain layer 63 that has at least one component of the diffusion that is aligned to an edge of the oxide 53 that extends horizontally over the region of the first diffusion. This is discussed in more detail in the present specification at least starting at page 11, line 4. As noted above, the metal lines are in direct contact with the sidewall film, and thus this feature is not found in the cited reference.

Specifically, the cited reference neither describes nor suggests at least the combination of features of "... *said gate electrode and said insulating film defining lightly doped first drain and source layers* ...", as recited in independent claim 1, as amended herein. The dependent claims are felt to be patentable at least as depending upon a base claim shown above to be patentable. Therefore, applicant respectfully requests that this rejection be withdrawn.

The rejection of claims 3-4, 6, 9-10 and 22 under 35 U.S.C. 103(a) as being unpatentable over Gonzales in view of Cheng is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that claims 3-4, 6, 9-10 and 22 are neither disclosed nor suggested by the references taken separately or in combination.

The cited reference of Gonzales is discussed above. The features of the independent claims are also discussed above. The features of the cited reference of Cheng include an insulated gate semiconductor device having gate electrodes, and including source region 57 and drain region 58, source region 59 and drain region 62. Openings in a layer of dielectric material 63, expose portions of the S/D regions 57, 58, 59, and 62, and portions 28 and 29 of gate electrodes 35 and 35'. Silicide 64 is formed on the exposed S/D regions 57, 58, 59, and 62 and on the exposed portions of 35 and 35'. An insulating layer 66 is formed on layers 63 and 64. Openings formed in the layer 66 expose portions of layer 64. Dopant regions 57 and 58 are formed having a concentration

ranging from $1x10^{19}$ atoms/cm^3 to approximately $5x10^{20}$ atoms/cm^3. Dopant regions 43 and 44 have concentrations ranging between $1x10^{16}$ to $5x10^{17}$ atoms/cm^3.

Applicant's amended independent claim 1, from which claims 3-4 depend, is neither described nor suggested by the suggested combination of Cheng with Gonzales, since neither reference discloses nor suggests the combination of features of "*...said at least one sidewall having a sidewall offset extending outwardly of said gate electrode along a horizontal surface of said semiconductor substrate in at least one of regions below which at least one of said second drain and source diffusion layers are to be formed, said sidewall offset extending along a lateral surface of a gate oxide film on which said gate electrode is formed by an amount that is greater than a vertical thickness of said sidewall....*" as set forth in applicant's amended claim 1.

As noted above with reference to the rejection over Gonzales, the cited reference does not disclose a sidewall offset that defines the surrounded diffusions. Cheng discloses an insulating layer 66 formed on a layer of dielectric material and silicide 64, but neither describes nor suggests a sidewall offset that extends along a surface of a gate oxide film by an amount that is greater than the thickness of the sidewall film, as found in applicant's amended independent claim 1, as discussed previously. The reason that this is so is that the cited references define the sidewall location and extent by means of a non masked anisotrophic timed etch process that does not allow for a lateral offset such as found in the present claimed invention.

Applicant's claim 6 is also neither disclosed nor suggested by Cheng for reasons similar to those set forth regarding amended claim 1. Therefore, since the independent claims are not obvious over the suggested combination of cited references, then the dependent claims 3-4, 6 9-10 and 22, which contain further patentable features over the base claim, also can not be rendered obvious by the suggested combination of cited references. Therefore, applicant respectfully requests that this rejection be withdrawn.

The rejection of claim 7 under 35 U.S.C. 103(a) as being unpatentable over Gonzales in view of Cheng, and further in view of Kunishima, is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that claim 7 is neither disclosed nor suggested by the suggested combination of cited references, whether taken separately or in any combination.

The Gonzales and Cheng references are discussed above, as are the features of the independent claims of the present application. The cited reference of Kunishima discloses a semiconductor FET device with a SiO2 film 23 and a BPSG film 25 sequentially deposited on top of a substrate that is lamp annealed to increase the concentration of the p+ type impurity diffusion layer 17, as shown in Figure 5C. There is also a $TiSi_2$ layer 21 shown in Figure 5C, and discussed at column 10, lines 16-59. Figure 5A shows a gate oxide film 5 and a gate electrode having stacked films, which is discussed at column 9, lines 32-35. Dependent claim 7, which depends from claim 6, recites that the low resistive wiring layers are composed of TiSi.

Applicant respectfully submits that the cited reference of Kunishima adds nothing significant to the other cited references in that Kunishima also neither discloses nor suggests a semiconductor device that includes a sidewall offset extending along a surface of a gate oxide film on which the gate electrode is formed, as set forth in applicant's amended claim 6, from which dependent claim 7 depends. The cited reference of Kunishima has a gate oxide film 5, a gate electrode, and an SiO2 film 23 and a BPSG film 25 sequentially deposited on top of a substrate. However, as discussed previously, Kunishima does not suggest a sidewall offset that extends along a surface of a gate oxide film on which the gate electrode is formed, as found in the present claimed invention.

Applicant respectfully submits that the dependent claim 7, is patentable at least as depending upon a base claim shown above to be patentable. In view of the foregoing, applicant respectfully requests that this rejection be reconsidered and withdrawn.

The rejection of claims 1-4, 6, 8-10, 21 and 23 under 35 U.S.C. 103(a) as being unpatentable over Cheng, is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that claims 1-4, 6, 8-10, 21 and 23 are neither disclosed nor suggested by the cited reference, whether taken alone, or in any combination with well known art. Claim 1 is summarized above. Claims 2-4 depend from claim 1. Claim 6 is summarized above. Claims 8-10, 21 and 23 depend from claim 6. The cited reference of Cheng is discussed above.

For reasons similar to those set forth elsewhere herein, applicant respectfully submits that independent claims 1 and 6 are neither disclosed nor suggested by Cheng, whether taken alone, or in any combination with other known references. Specifically, the suggested reference of Cheng neither describes nor suggests the combination of features of a sidewall offset extending along a surface of a gate oxide film on which said gate electrode is formed, as found in the claimed invention as previously discussed. Cheng discloses a sidewall 38, but does not suggest that the sidewall extends along the surface to limit the location the diffusions. The reference does not discuss the problem addressed by the claimed invention, and uses the prior art approach to provide an edge definition for the silicide process. Thus the independent claims 1 and 6, as amended herein, and thus the dependent claims based upon them, are non obvious over Cheng.

In view of the foregoing, applicant respectfully requests that this rejection be withdrawn.

The rejection of claims 5, 7, 11, 21 and 23 under 35 U.S.C. 103(a) as being unpatentable over Cheng in view of Kunishima, is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that claims 5, 7, 11, 21 and 23 are neither disclosed nor suggested by the suggested combination of cited references, whether taken alone, or in any combination.

The Cheng and Kunishima references are discussed above. The features of the independent claims upon which dependent claims 5, 7, 11, 21 and 23 are based are also discussed above.

Applicant respectfully submits that the cited reference of Kunishima adds nothing to the other cited reference of Cheng, as discussed above, in that Kunishima also neither discloses nor suggests a semiconductor device that includes a sidewall offset extending along a surface of a gate oxide film on which the gate electrode is formed, as set forth in applicant's amended independent claims, from which dependent claims depend. The addition of a silicide layer is seen as adding nothing to the disclosure of Cheng, which was shown above to not render the independent claims obvious.

In view of the above discussion, applicant respectfully requests that this rejection, as set forth in the Office Action, be reconsidered and withdrawn.

Based on the above, applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-951-6676.

Respectfully submitted,
HUTCHINS, WHEELER & DITTMAR

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Date

Donald W. Muirhead
Reg. No. 33,978

Patent Group
Hutchins, Wheeler & Dittmar
101 Federal Street
Boston, MA 02110